ADDRESS CONTROL FOR EFFICIENT MEMORY PARTITION

ABSTRACT OF THE DISCLOSURE

A memory cell of a programmable device includes a memory partitioning circuit to partition a multiple port memory device into one or more single port memory partitions. The memory partitioning circuit prevents cross addressing by setting the value of one or more address lines of each memory port to a fixed value. The memory partitioning circuit holds address lines at their required values during the programmable device's normal, clear, and reset modes of operation. The behavior of the memory partitioning circuit is set by a portion of a device configuration used to configure the programmable device. The memory partitioning circuit is connected between a memory cell's address register and row or column decoders used to access the multiple port memory device. The memory partitioning circuit can also perform bit-wise inversion operations on portions of the memory addresses.

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